In the Specification:

Please add the following paragraph after paragraph [0031] in the Brief Description of the Drawings.

Figures 9a and 9b are cross-sectional views showing a planarization material.

Please amend paragraph [0008] as follows:

[0008] The simplest example of a multiple-gate transistor is the double-gate transistor, as described in U.S. Patent No. 6,413,802 issued to Hu, et al. U.S. Patent No. 6,413,802 is incorporated herein by reference. As illustrated in a cross-sectional view in Figure 2a, the double-gate transistor 100 has a gate electrode 106 that straddles across the channel within the fin-like silicon body 102, thus forming a double-gate structure. There are two gates, one on each sidewall 108 of the silicon fin 102, and separated from the fin 102 by gate dielectric [[100]] 110. An etchant mask 112 overlies a top surface of fin 102. The plan view of the double-gate structure is shown in Figure 1.

Please amend paragraphs [0010–0012] as follows:

[0010] Another example of the multiple-gate transistor is the triple-gate transistor. A cross-section of the triple-gate transistor [[100]] 100' is illustrated in Figure 2b and thus the plan view of the triple-gate structure is the same as the double gate structure shown in Figure 1. The triple-gate transistor structure [[100]] 100' has a gate electrode 106 that forms three gates: one gate on the top surface 116 of the silicon body/fin 102, and two gates on the sidewalls 108 of the silicon body/fin 102. The triple-gate transistor achieves better gate control than the double-gate transistor because of it has one more gate on the top of the silicon fin.

[0011] The triple-gate transistor structure may be modified for improved gate control, as illustrated in Figure 2c. Such a structure [[100]] 100'' is also known as the Omega (Ω) field-

effect transistor (FET), or simply omega-FET, since the gate electrode 106 has an omega-shape in its cross-sectional view. The encroachment of the gate electrode 106 under the semiconductor fin or body 102 forms an omega-shaped gate structure. This encroachment results in notch or undercut region [[132]] 118 as shown in Figure 2c. It closely resembles the Gate-All-Around (GAA) transistor for excellent scalability, and uses a very manufacturable process similar to that of the double-gate or triple-gate transistor.

[0012] The omega-FET has a top gate, adjacent surface 110, two sidewall gates, adjacent sidewalls 108, and special gate extensions or encroachments 118 under the fin-like semiconductor body 102. The omega-FET is therefore a field effect transistor with a gate electrode 106 that almost wraps around the body. In fact, the longer the gate extension, i.e., the greater the extent of the encroachment *E*, the more the structure approaches or resembles the gate-all-around structure. The encroachment of the gate electrode 106 under the silicon body 102 helps to shield the channel from electric field lines from the drain and improves gate-to-channel controllability, thus alleviating the drain-induced barrier lowering effect and improving short-channel performance.

Please amend paragraph [0014] as follows:

[0014] Figure 3 shows a prior art process for forming a gate electrode 106 in a multiple-gate transistor. In Figure 3a, a gate electrode material 120 is deposited over a semiconductor fin 102 and covered with a gate dielectric [[104]] 110. As shown, the top surface of the gate electrode material 120 is non-planar due to the fin 102.

Please amend paragraph [0035] as follows:

[0035] A method of forming a gate electrode of the multiple-gate transistor is illustrated using the flow chart of Figure 4. Three-dimensional perspectives of the multiple-gate transistor during the various process steps described in Figure 4 are illustrated in Figures 5a-5i. The

formation of device 200 begins with a semiconductor-on-insulator substrate that includes a semiconductor layer 202 overlying an insulator layer 204, as shown in Figure 5a. The insulator layer 204 overlies a substrate 206. The semiconductor layer 202 may be formed from an elemental semiconductor such as silicon, an alloy semiconductor such as silicon-germanium, or a compound semiconductor such as gallium arsenide or indium phosphide. The semiconductor layer [[206]] 202 is preferably silicon. The thickness of the semiconductor layer may be in the range of about 200 angstroms to about 5000 angstroms. In an alternate embodiment, bulk semiconductor substrates such as a bulk silicon substrate may also be used.

Please amend paragraph [0045] as follows:

[0045] Referring next to Figure 5e, a chemical mechanical polishing (CMP) process is performed to planarize the top surface of the second gate electrode material 216. The CMP process may or may not expose the first gate electrode material 214. In Figure 5e, the CMP process does not expose first gate electrode material 214. Figure 8 is provided to show the case where the first gate electrode material 214 is exposed. The root-mean-square surface roughness of the planarized top surface of the gate electrode material [[216]] 212 is preferably less than 100 angstroms.

Please amend paragraph [0046] as follows:

[0046] The definition of gate electrode 220 (see Figure 5i) will now be described with respect to Figures [[5e-5g]] 5e-5i. A mask material 222 is formed on the substantially planarized top surface of the gate electrode material 216, as shown in Figure 5f. The mask material 222 is then patterned to create a patterned mask 224 as shown in Figure 5g. As a result of the substantially planarized top surface, a desired predefined pattern can be accurately transferred onto the mask material 222 to form a patterned mask 224.

Please amend paragraphs [0049–0052] as follows:

[0049] The patterned mask 224 may then be removed as shown in Figure 5i. The portion of the gate dielectric 210 not covered by the gate electrode [[212]] 220 may or may not be removed during the etching process. In the case where some gate dielectric remains on the semiconductor fin 208 not covered by the gate electrode [[212]] 220, the gate dielectric 210 may be subsequently removed by dry or wet etching.

[0050] The process of Figures 5a-5i illustrated the formation of a triple-gate transistor device. It is understood that similar process steps could be used to form any other multiple gate transistor. For example, an etchant mask (see element 112 in Figure 2a) can be formed over the semiconductor fin 208. Similarly, the insulating layer 204 can be recessed, resulting in a notch (see element [[132]] 118 of Figure 2c) at the base of the semiconductor fin 208. Any of the other features incorporated in Figures 2a, 2b and 2c could similarly be incorporated in a device of the present invention.

[0051] Referring now to Figure 6, the source and drain regions may then be formed. The formation of the source and drain regions may involve many steps. In the preferred embodiment, an ion implantation process is first performed to dope the source and drain regions 228 and 230 immediately adjacent to the channel region. The channel region is the portion of the semiconductor fin 208 wrapped around by the gate dielectric 210 and the gate electrode [[212]] 220.

[0052] Spacers 226 are then formed on the sidewalls of the gate electrode [[212]] 220. The spacers 226 may be formed by deposition of a spacer material followed by anisotropic etching of the spacer material. The spacer material comprises of a dielectric material, preferably silicon nitride but alternately silicon oxide or another insulating material. The spacer material may also be comprised of a stack of dielectric materials, such as a silicon nitride layer overlying a silicon oxide layer.